

Figure 1

Phase Alignment  
Process

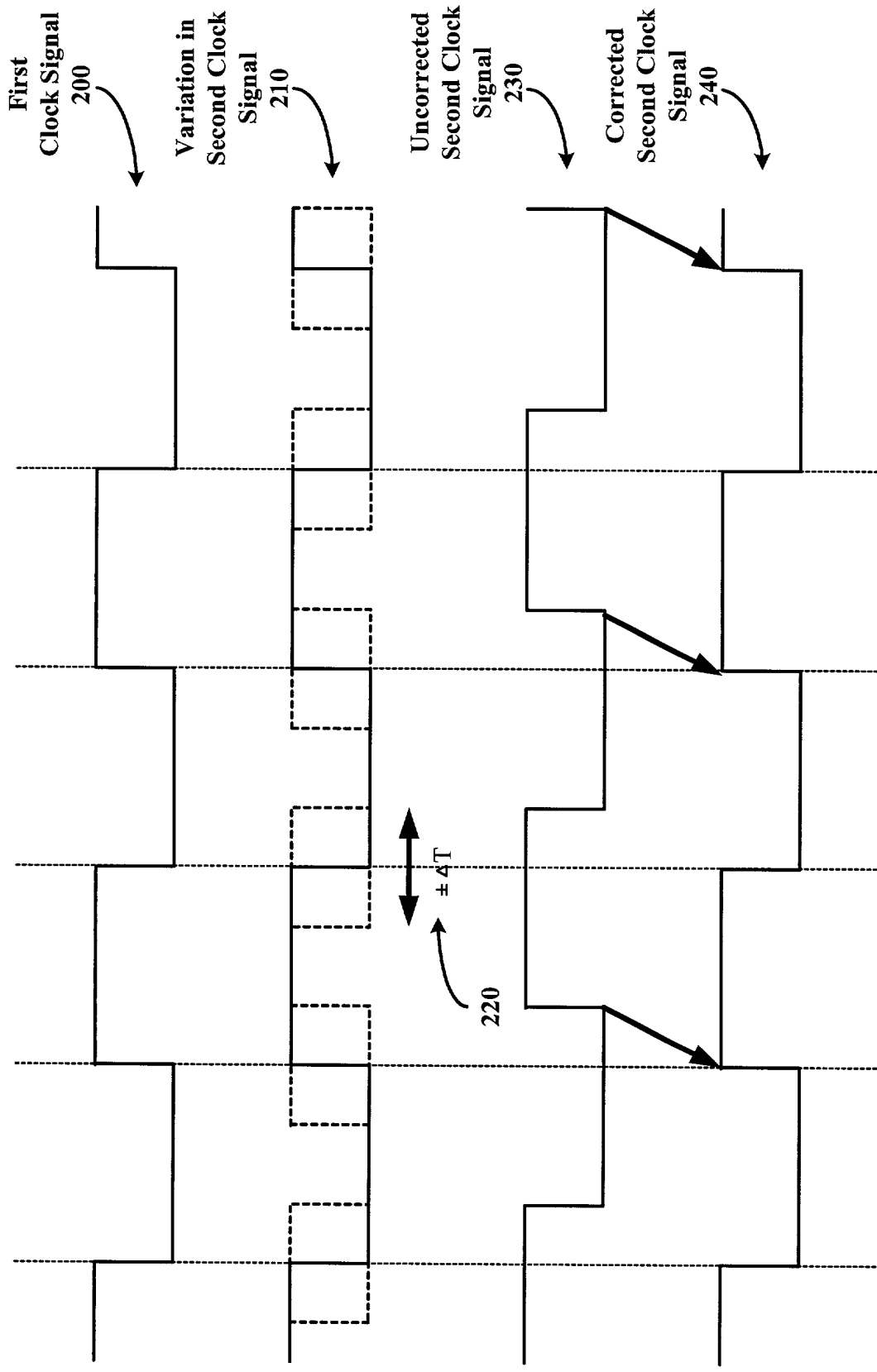


Figure 2

Phase Alignment  
of Clock Signals

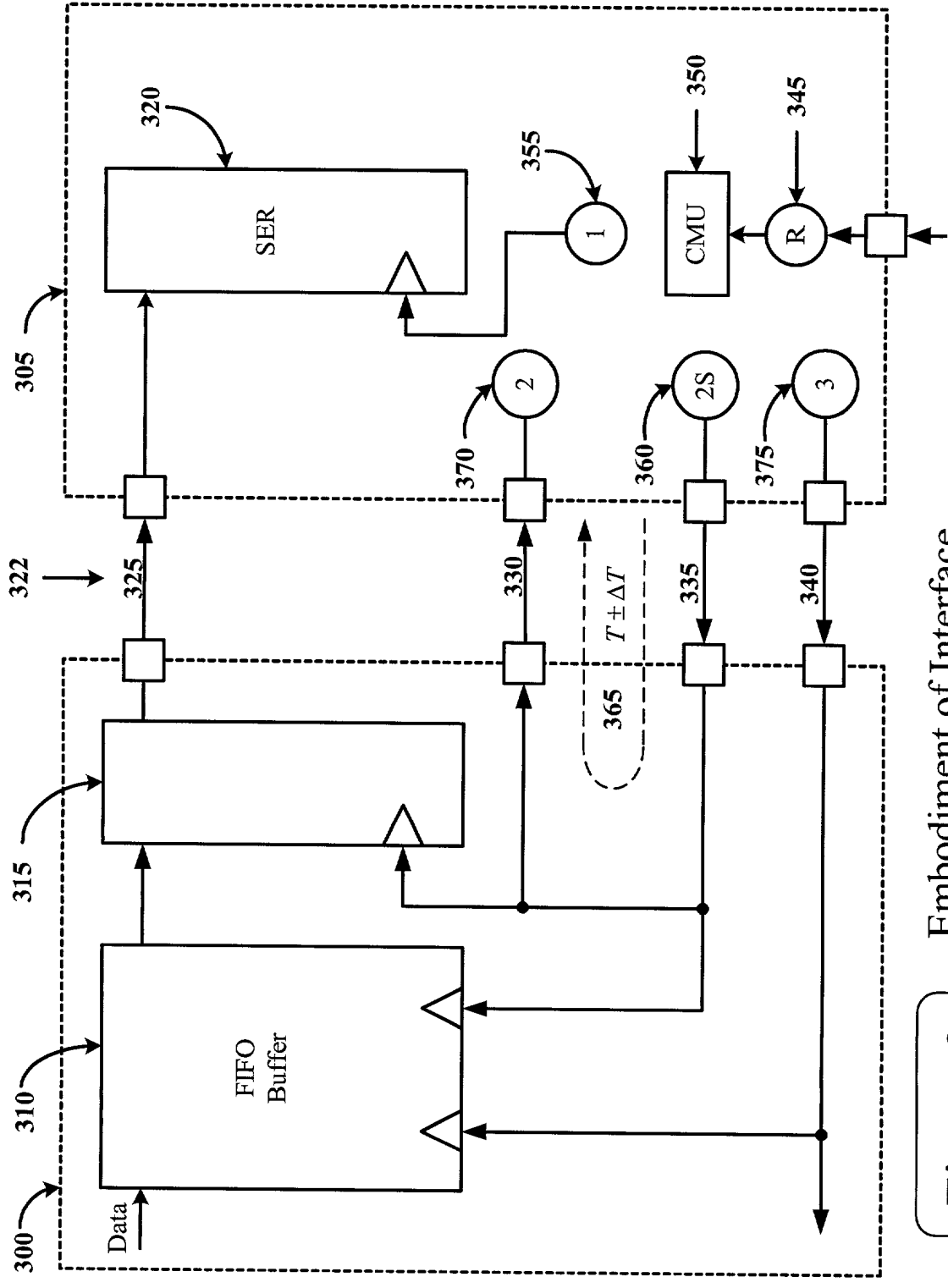
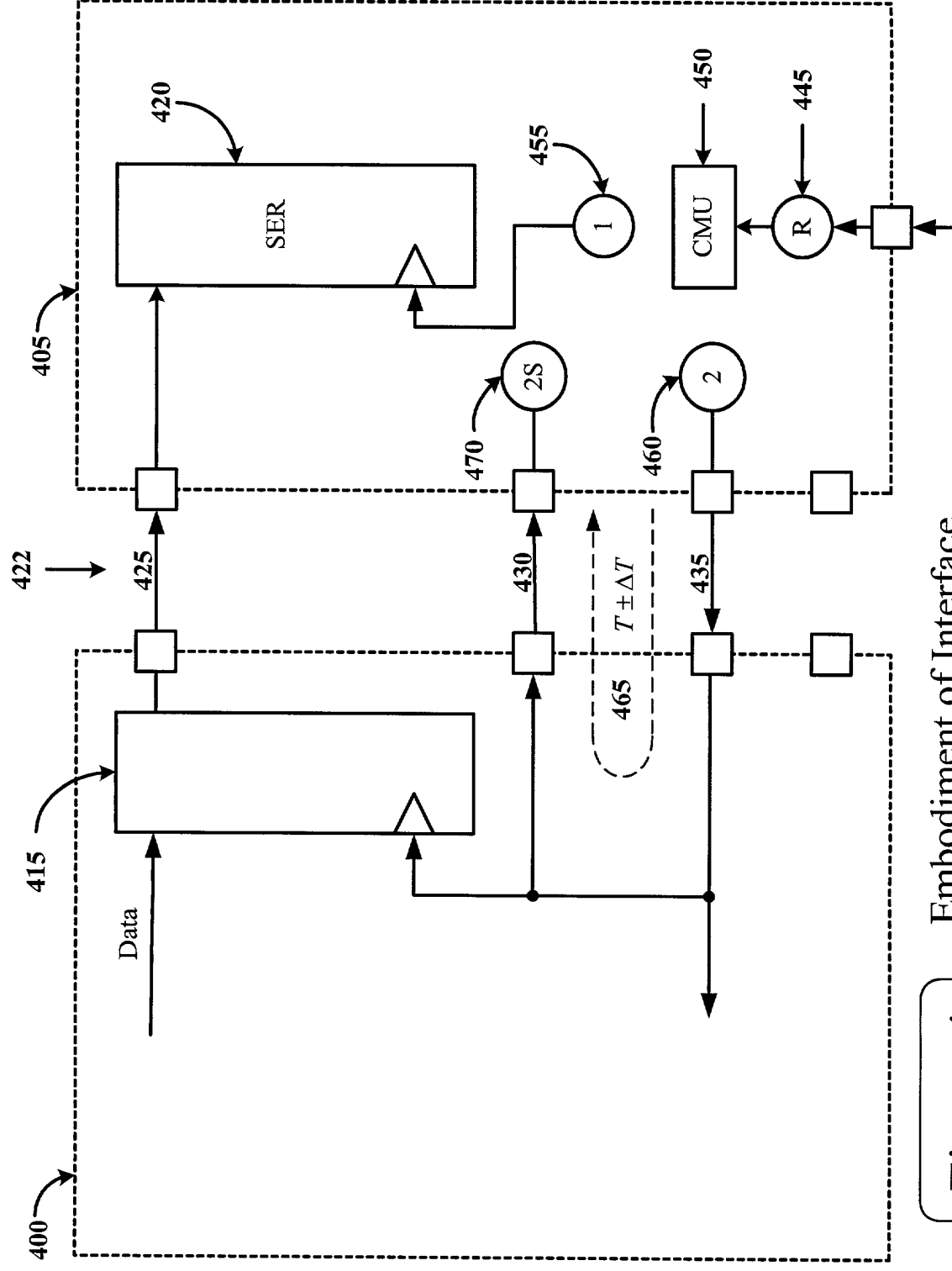


Figure 3  
Embodiment of Interface  
With FIFO Buffer



Embodiment of Interface  
Without FIFO Buffer

Figure 4